CADU Frame Synchronization

CADU frame synchronization is performed by sliding a window of 32 bits and checking the sequence against the CADU packet header. If a bit sequence that matches the header is found, then frame synchronization is declared. In an ideal world, one would force all 32 bits to match the CADU header sequence in order to declare that the frame is synched and valid, however, this could cause many packets to be missed under high noise conditions. It is important to set a suitable frame-synchronization threshold (lower than 32 bits).

Let the number of differences between the header sequence and a portion of the data sequence be denoted by

$$s = \sum xor(\vec{r}(1,\ldots,32), 0x1ACFFCID)$$

The 32-bit section of the data sequence that is being evaluated for frame-synchronization is represented as $\vec{r}(1,\ldots,32)$. The summation represents the total number of differences between the 32 bit section of processed data and the ideal header. For instance, if the 32 bit section of data differs in 5 of 32 places from 0x*1ACFFCID*, then $s = 5$. A frame is detected or missed based on the value of *s* and the frame-synchronization threshold: th.

$$\begin{aligned} \textit{Frame Synch Found:} \quad & s \le th \\ \textit{No Frame Present:} \quad & s > th \end{aligned}$$

Over extremely adverse channels, some frame headers have $s = 20$ (which ultimately means that 20 out of 32 bits in the header are incorrect), yet the packet can still be decoded after RS decoding. To handle such cases, there are four states of frame-synchronization lock. The value th varies based on the lock-state.

Lock State-0 is defined as being completely unlocked, and thus has the most stringent frame synchronization threshold requirement to prevent a false detection. On the other hand State-3 is defined as being ideally locked, and thus the least stringent threshold. On Figure 1 a synchronization state machine diagram is shown. Each state has a lock status number and its associated frame-synch threshold. The figure also shows the transition cases to go from one state to the next.

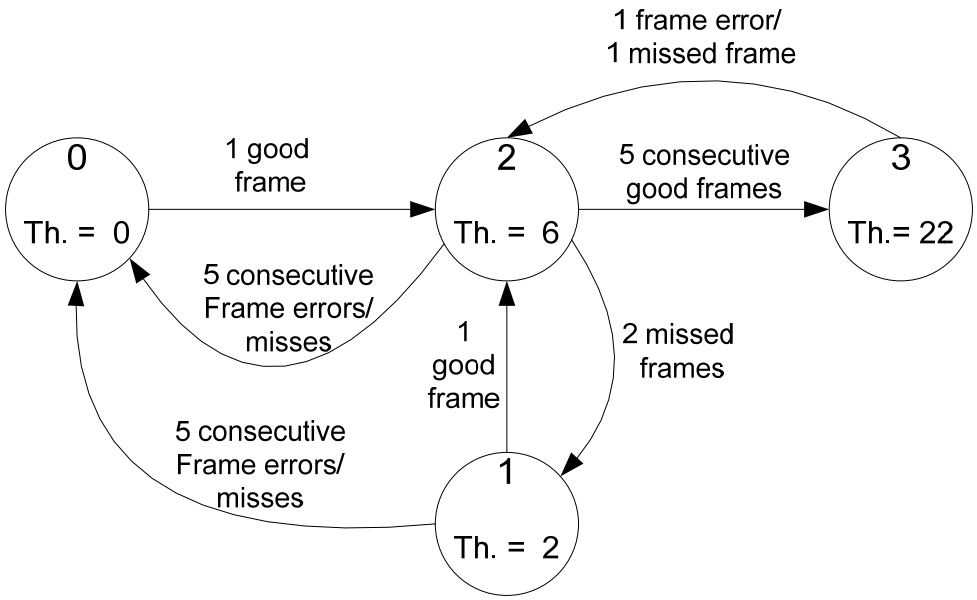

Figure 1: CADU Frame Synchronization Lock State Graph

The lock state remains unchanged until an event happens that causes a state transition. The receiver begins in State-0, and thus the 32-bit sequence must perfectly match the CADU header to declare a frame-synch. This stringent requirement remains in place until a frame is found and successfully decoded without error. From there, the state machine goes immediately to State-2. In this state, we assume that successive headers can be found with exact synchronization, i.e., exactly 1024 bytes away from the previous header. While in State-2, if five consecutive frames are found with uncorrectable errors in all five frames, then State-2 is downgraded back to State-0. If five consecutive frames are detected and decoded error-free, then the state machine is upgraded to State-3.

State-3 assumes that you are perfectly locked, and thus the threshold of tolerable errors is set to a very high number. The default number of tolerable errors in the header for this state is set to 22. The user can set its desired threshold for State-3 by setting the flag "–thresh x" at the command prompt, where "x" is the desired threshold. A command of "–thresh 32" would guarantee that all packets are forwarded to the RS decoder when in State-3. If a frame isn't found, then the lock state is downgraded to State-2.

Synchronization can be lost unexpectedly for a number of reasons, including RF impairments such as an abrupt frequency drift, fades in the received signal, etc. It is common for a packet to appear unlocked in severe noise conditions (due to excessive errors in the header sequence) but this does not always imply that the software receiver has lost lock. This is the reason why, for State-3, the threshold is set to a very high value to ensure that lock is maintained in high noise conditions. The State-machine can still detect when lock is truly lost

since as soon as a single frame is found to be in error, State-3 is immediately downgraded to State-2, and from there, it can easily restart the state machine and go back to State-0.

When in State-2 or 3, the next frame in the transmission should be exactly 1024 bytes away. If a frame is not found exactly 1024 bytes ahead of the previous frame header, then the software radio advances 1024 bytes and searches for the next header in the exact location is expects to find it. No attempt is made to search in the middle of a frame while in-lock since it would reduce throughput and increase the chance of locking to a false header. If headers cannot be found in the positions they are expected to be in, the state machine moves to State-1.

The threshold in State-1 has a threshold of two errors allowed. With the threshold set to such a stringent level, it is safe to search byte by byte (in the middle of a packet) to try to find the next header. After scanning 3072 bytes (three packets) without success, the state machine assumes it lost all time reference and returns to State-0 to begin all over again. Note that two missed frames are pre-requisite to entering State-1, thus if an additional three frames are missed in State-1, then five total consecutive frames have been missed.

There is one additional caveat to the state diagram. The EMWIN-N signal has a differential decoder which removes the polarity ambiguity; however the LRIT signal does not have such a feature. When the LRIT receiver is in State-0, it will alternatively try to synch to the assumed header and its inverted (180°) version.

RS Decoding

Once the CADU frames are synched, they are sent to the (223,255)-RS decoder. As shown in Figure 15, the CADU payload contains 1020 bytes of data. The 1020 bytes are comprised of four interleaved RS frames of 255 bytes each. The RS decoder de-interleaves the four RS frames and checks to see if each of the four syndromes are correct. If one of the frames is in error, the entire CADU packet is dropped.